PENDING CLAIMS AND STATUS THEREOF

1. **(currently amended):** A method of processing an interruptible repeat instruction, comprising:

setting a repeat flag;

fetching a target instruction for repeated execution;

executing the target instruction a predetermined number of times; **[[and]]**

interrupting the executing during a processing exception to load a first instruction from an interrupt service routine into an instruction register for subsequent execution, the first instruction being determined without reference to a program counter**; and**

continuing the executing after the interrupting when the repeat flag is set without re-fetching the target instruction.

2. (original): The method according to claim 1, further comprising:

fetching a repeat instruction that determines the target instruction for repeated execution.

3. (original): The method according to claim 2; wherein the repeat instruction includes a loop count value that determines the predetermined number of times the target instruction is executed.

4. (original): The method according to claim 2, wherein the repeat instruction includes an address specifying a memory location that includes a loop count value for determining the predetermined number of times the target instruction is executed.

Claims 5-7 (canceled)

8. (original): The method according to claim 1, further comprising resetting the repeat flag after executing the target instruction the predetermined number of times.

9. **(currently amended):** A processor including interruptible repeat instruction processing, comprising:

a program memory for storing instructions including a repeat instruction and a target instruction;

a program counter for identifying current instructions for processing;

a loop control unit for executing the repeat instruction to a) store and change a loop count value in a repeat count register and b) prevent an instruction after the target instruction from being fetched until the loop count value reaches or exceeds a predetermined value; and

an execution unit for repeatedly executing the target instruction until the loop count value reaches or crosses the predetermined value;

wherein the executing ~~may be~~ **is able to be** interrupted during a processing exception to load a first instruction from an interrupt service routine into an instruction register for subsequent execution, the first instruction being determined without reference to a program counter.

10. (original): The processor according to claim, wherein the repeat instruction itself includes the loop count value.

11. (original): The processor according to claim 9, wherein the repeat instruction includes an address specifying a memory location that includes the loop count value.

12. (original): The processor according to claim 10, further comprising:

a status register;

wherein the loop unit further sets a repeat flag within the status register during repeat instruction processing.

13. (original): The processor according to claim 12, wherein the execution unit continues to repeatedly execute the target instruction after the interrupt when the repeat flag is set.

14. (original): The processor according to claim 12, wherein the loop control unit resets the repeat flag after the loop count value reaches the predetermined value.

15. (original): The processor according to claim 9, wherein the loop control unit changes the loop count value by decrementing it.

16. (original): The processor according to claim 9, wherein the loop control unit changes the loop count value by incrementing it.

17. (original): The processor according to claim 9, wherein the predetermined value is zero.

18. (original): The processor according to claim 9, wherein the predetermined value is not zero.